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P01/7700 0.00-0224133.9

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2. Patent application number
(The Patent Office will fill in this part) — 17 OCT 2002 — 0224133.9

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

TOUMAZ TECHNOLOGY LTD
THE INNOVATION CENTRE
BUILDING D5, CULHAM SCIENCE CENTRE
ABINGDON
OXFORDSHIRE
OX14 3DB

Patents ADP number *(if you know it)* 8098428001

If the applicant is a corporate body, give the country/state of its incorporation — UNITED KINGDOM

4. Title of the invention — ELECTRIC CIRCUIT

5. Name of your agent *(if you have one)* — Marks & Clerk

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

Sussex House
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4220 NASH COURT
OXFORD BUSINESS PARK SOUTH
OXFORD OX4 2RU

Patents ADP number *(if you know it)* 18004 01271125001

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Country	Priority application number *(if you know it)*	Date of filing *(day/month/year)*

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Number of earlier application	Date of filing *(day/month/year)*

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Claim(s)	3
Abstract	1
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MR P. J. ALLMAN
0161 233 5805

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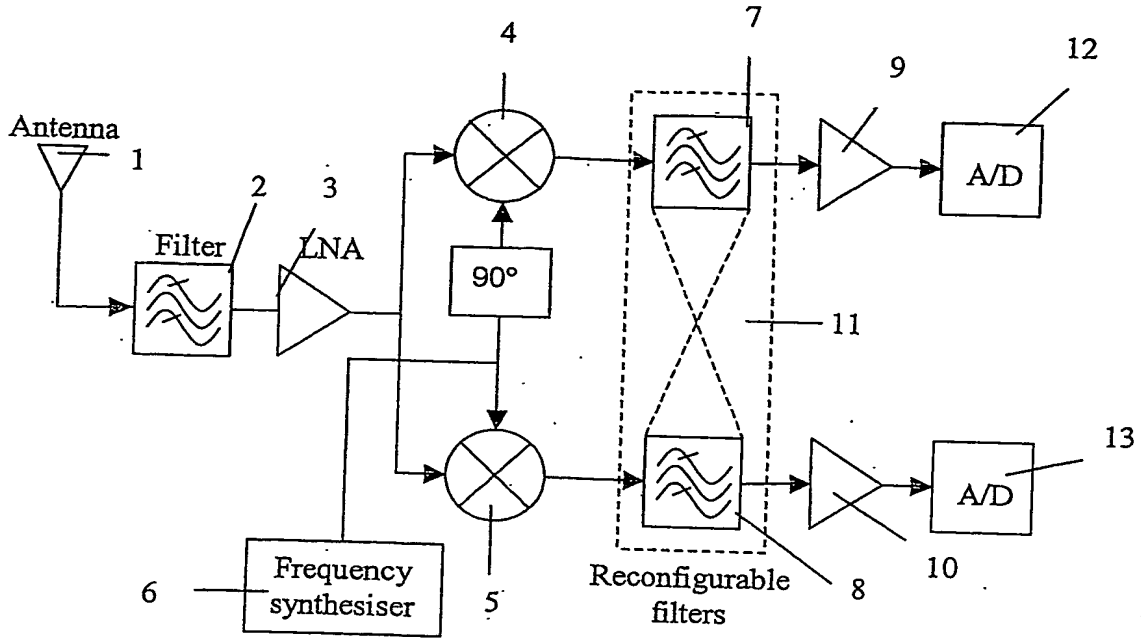

FIGURE 1

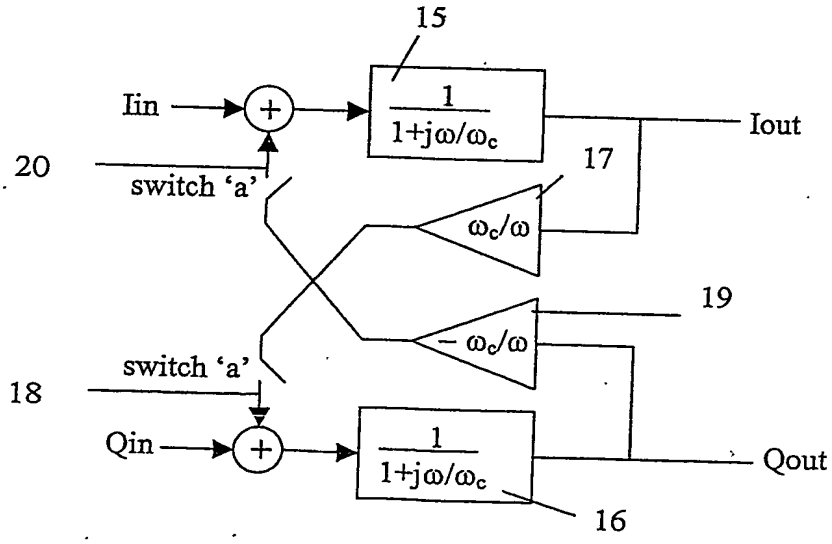

FIGURE 2

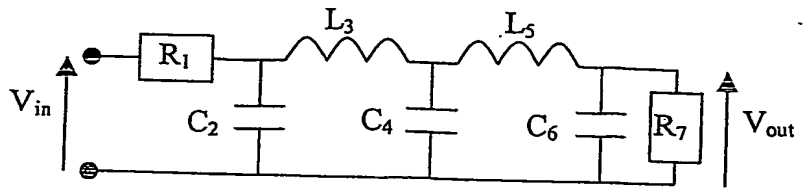

FIGURE 3

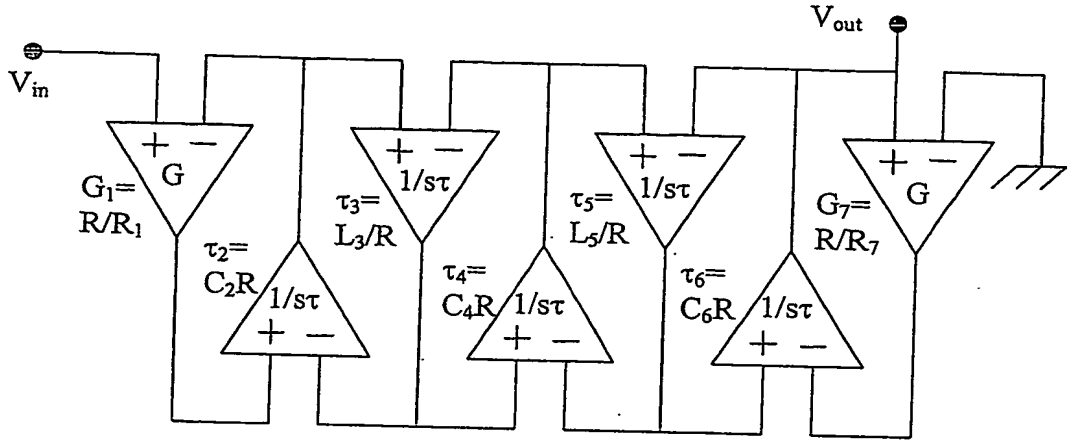

FIGURE 4

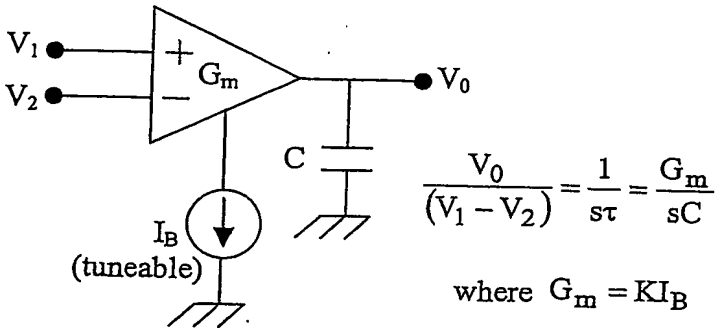

FIGURE 5

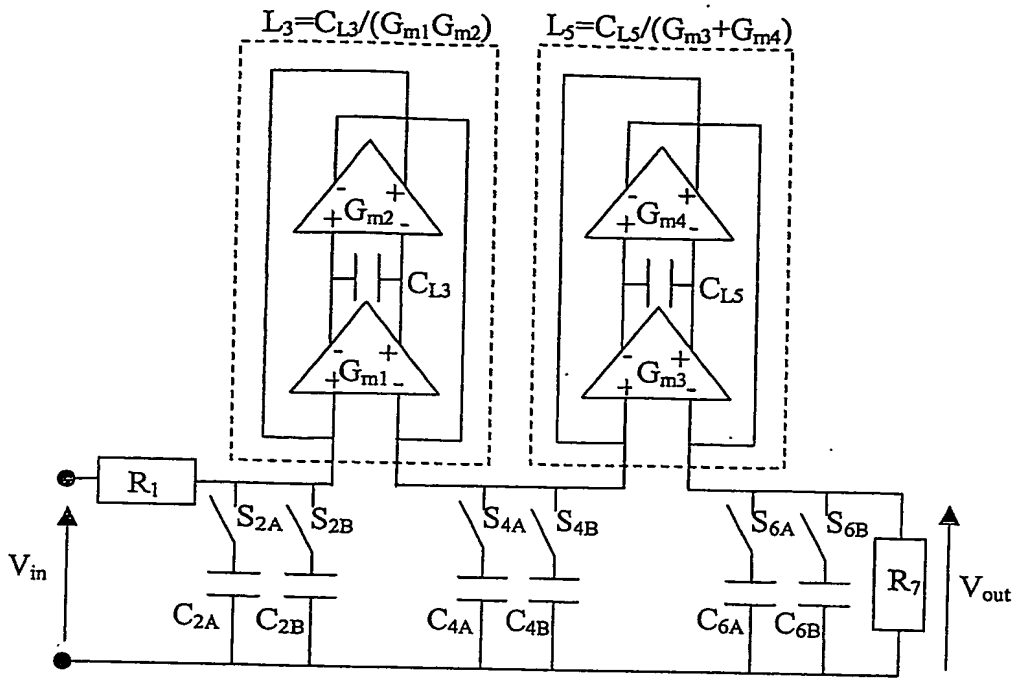
$L_3=C_{L3}/(G_{m1}G_{m2})$
$L_5=C_{L5}/(G_{m3}+G_{m4})$
G_{m2}
C_{L3}
G_{m1}
G_{m4}
C_{L5}
G_{m3}
R_1
S_{2A}
S_{2B}
S_{4A}
S_{4B}
S_{6A}
S_{6B}
V_{in}
C_{2A}
C_{2B}
C_{4A}
C_{4B}
C_{6A}
C_{6B}
R_7
V_{out}

FIGURE 6

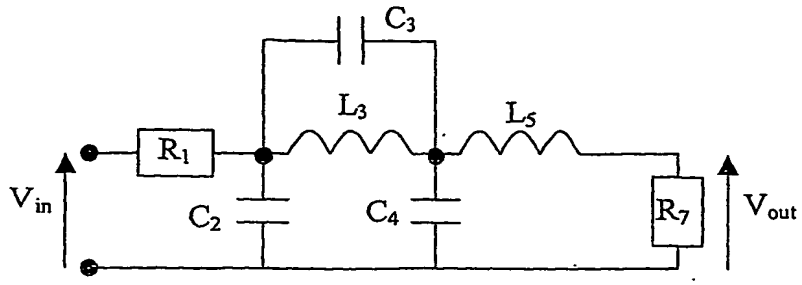

FIGURE 7

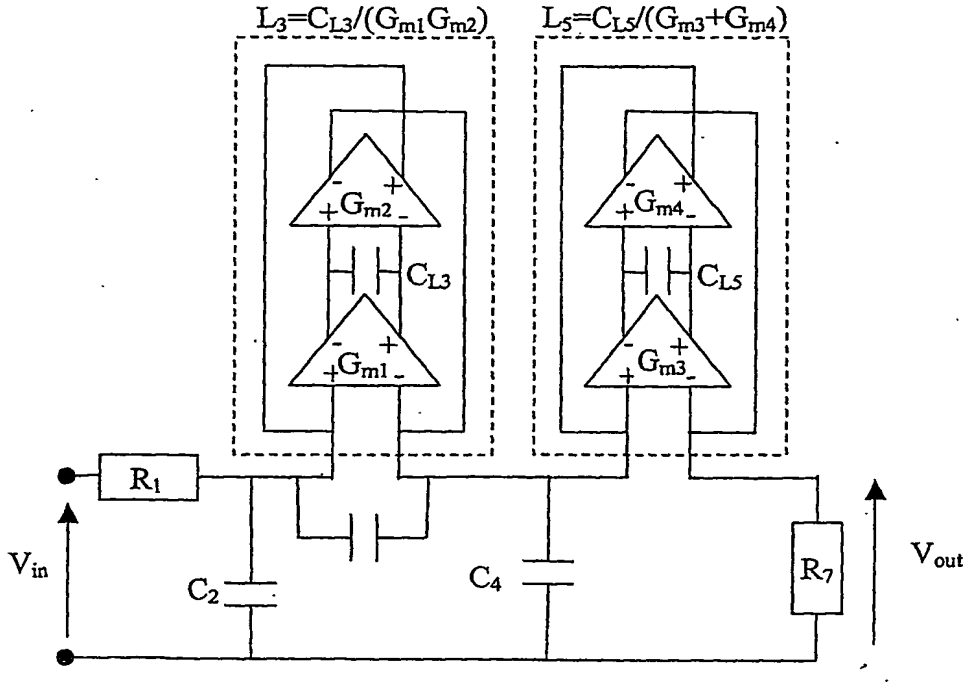

FIGURE 8

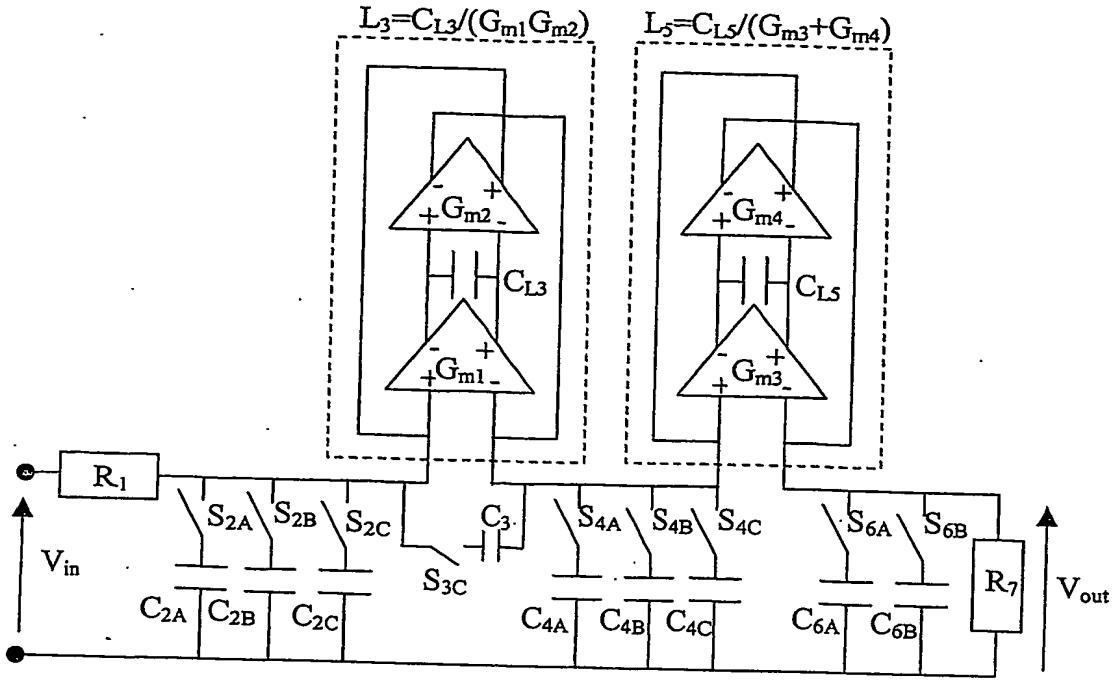
$L_3=C_{L3}/(G_{m1}G_{m2})$
$L_5=C_{L5}/(G_{m3}+G_{m4})$
G_{m2}
C_{L3}
G_{m1}
G_{m4}
C_{L5}
G_{m3}
R_1
V_{in}
S_{2A}
S_{2B}
S_{2C}
S_{3C}
C_3
S_{4A}
S_{4B}
S_{4C}
S_{6A}
S_{6B}
C_{2A}
C_{2B}
C_{2C}
C_{4A}
C_{4B}
C_{4C}
C_{6A}
C_{6B}
R_7
V_{out}

FIGURE 9

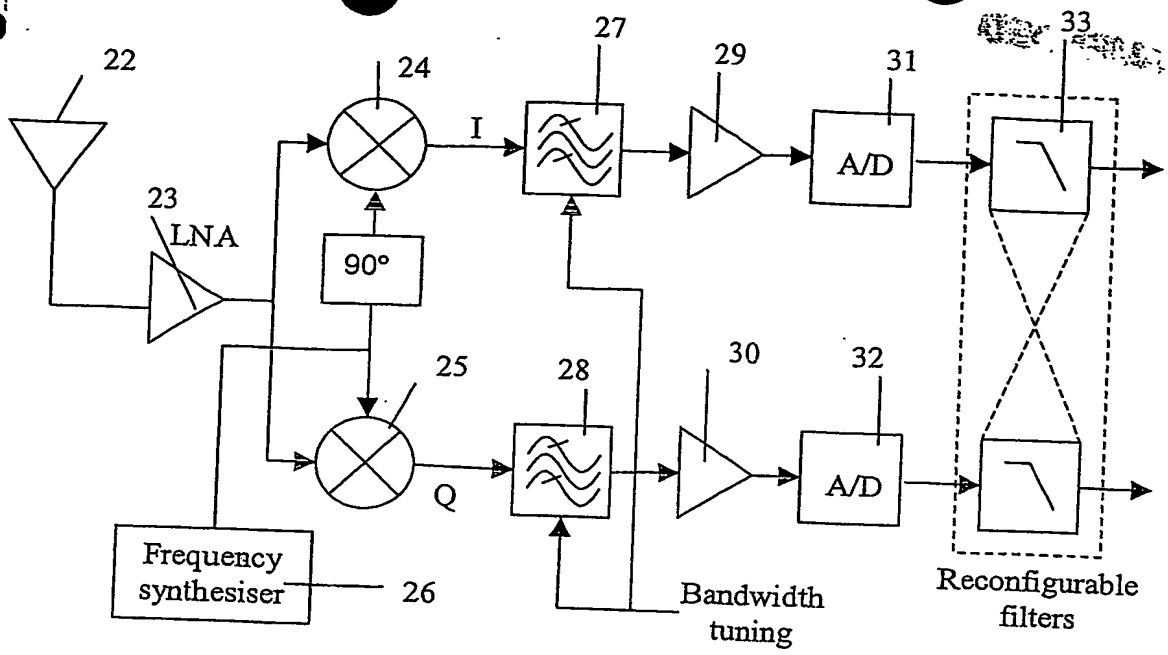

FIGURE 10

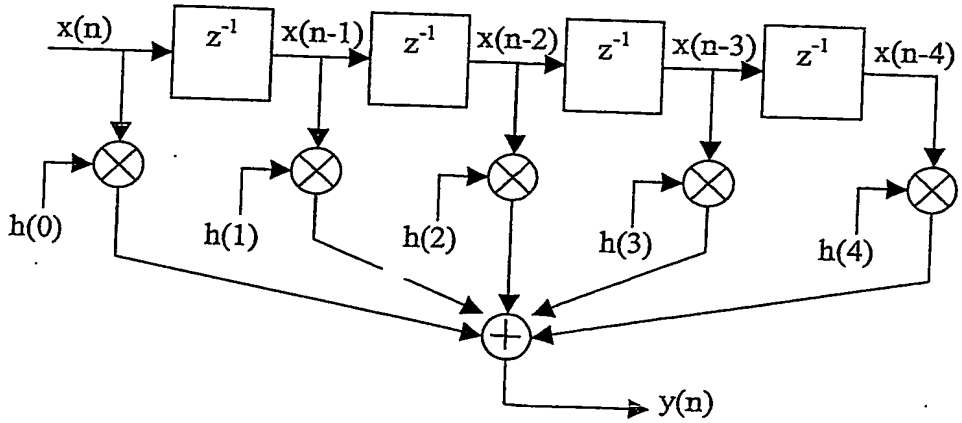

FIGURE 11

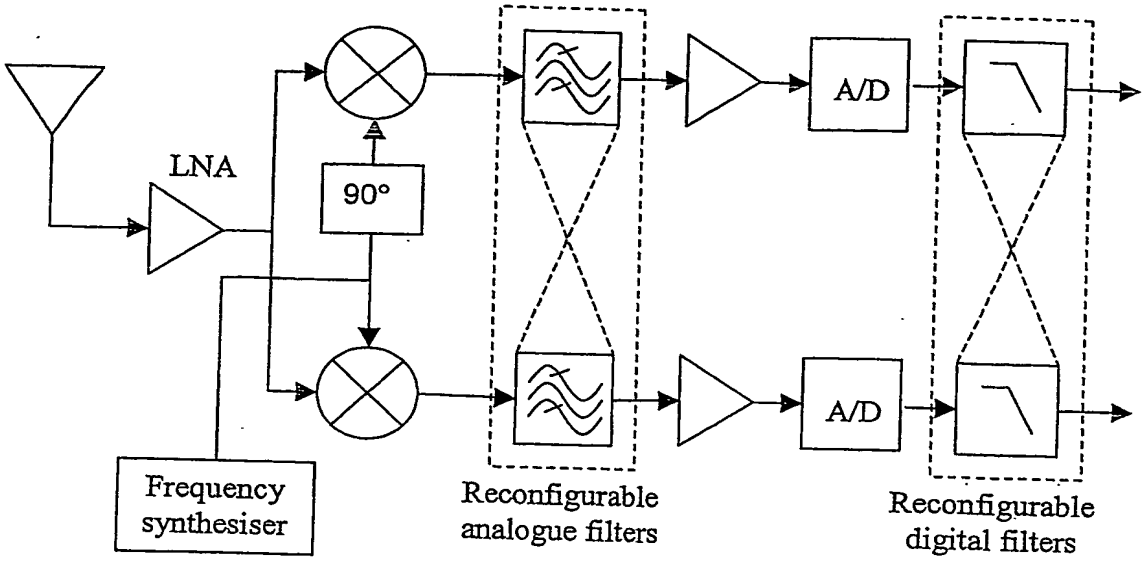
LNA
90°
A/D
A/D
Frequency synthesiser
Reconfigurable analogue filters
Reconfigurable digital filters

FIGURE 12

ELECTRIC CIRCUIT

The present invention relates to an electric circuit suitable for use as a radio receiver or as part of a radio receiver.

A proliferation of standards and modulation techniques for wireless communications has emerged in response to the particular requirements of different applications. These modulation schemes range from simple amplitude modulation (AM) and frequency modulation (FM) to complex multi-carrier digital modulation schemes such as wideband code-division multiple access (WCDMA) and coded orthogonal frequency domain multiplexing (COFDM). This proliferation in standards has led to the development of many different receiver architectures, which are optimised for specific applications.

A modern wireless communications receiver typically has two main parts, an analogue front-end, and a digital back-end. The digital back-end performs such functions as demodulation, decoding, error correction, etc. The analogue front-end typically down converts a particular wanted channel to a low enough frequency to enable it to be digitised, while ensuring that no corruption from adjacent channel signals occurs.

The analogue front-end can be considered as a 'black box' which takes a band of input signals, and converts the particular wanted channel down to a known frequency, referred to as the intermediate frequency (IF). There are various well-known analogue front ends, the most popular of these being the superheterodyne, zero-IF and low-IF. These front-ends are commonly referred to in the prior art as being "receivers" although they do not include digital back-ends. Thus the term "receiver" as used is the following text should not be taken to imply the presence of digital electronics; neither should it be taken to exclude the presence of digital electronics.

The superheterodyne receiver is widely used because it provides very high selectivity. An RF input signal is applied to a low noise amplifier (LNA) and is then fed to an

image reject (IR) filter which is typically implemented by a surface acoustic wave (SAW) filter. The signal output from the IR-filter is fed to a mixer where it is combined with a signal from a local oscillator (LO) to perform frequency downconversion to the intermediate frequency (IF). This IF signal is fed through an IF bandpass filter which performs channel selection based upon the IF. The IF filter is also typically implemented using a SAW filter.

The main issue in superheterodyne receiver design is the trade-off between image rejection and channel selection. If the chosen IF is high, the image signal will be greatly attenuated by the IR filter but adjacent channel suppression may not be good. Conversely if the IF is low the image will not be well attenuated although adjacent channels will be well-suppressed. The frequency plan in a superheterodyne receiver must thus be carefully chosen given the input signal frequency and adjacent channel conditions.

The superheterodyne receiver has very good selectivity (i.e. can accurately select the wanted channel and reject unwanted channels), but requires a number of very selective filters which can only be implemented as discrete (off-chip) components. These off-chip filters are typically power hungry, and so a superheterodyne receiver may not be the best solution for battery operated devices (i.e. devices which require very low power consumption). The off-chip filters will also increase overall system area and cost.

Zero-IF and low-IF receivers eliminate the need for off-chip filters, and thus are attractive for applications where low power consumption and high integration (minimum size) are important. These two receivers differ in the selection of the down converted intermediate frequency (IF).

For zero-IF, the centre of the wanted signal channel is placed at zero Hz. As a result, one half of the wanted signal channel is located in the positive frequency domain and the other half is in the negative frequency domain. Effectively, the two halves (sidebands) of the wanted signal channel 'overlap'. To avoid signal corruption, it is

necessary to use a quadrature receiver architecture with I and Q paths. The quadrature receiver architecture allows signal information to be recovered from the overlapping signal channel sidebands, by combining I and Q channel information. This is recovery is typically done by a digital back-end.

An advantage of the zero-IF receiver is that the wanted channel is converted very quickly to baseband (zero Hz), and thus only low frequency filters and amplifiers are needed on-chip (easy to design). In addition, although the signal channel sidebands overlap in I and Q paths, the signal is effectively interfering with itself, and so the 'interferer' power is the same as the 'wanted' power. However a major disadvantage is that any low frequency noise and offsets which are present in the receiver will directly corrupt the wanted signal channel, since it is centred at zero. In sub-micron CMOS technologies this low frequency noise can be quite significant.

In a low-IF architecture, the wanted channel is converted to a low frequency so that, as in zero-IF, the filters and amplifiers required are easy to design. However, the IF is chosen so that it is in a region where noise and offsets are not a problem. Consider a wanted signal at frequency f_{RF}. This signal is converted to the low IF f_{IF} by multiplying it with an oscillator signal $f_{LO} = f_{RF} - f_{IF}$. However there could well be another channel picked up by the antenna at a frequency $f_{IM} = f_{LO} - f_{IF}$. When this signal is multiplied by the local oscillator (LO) it will be converted to $-f_{IF}$, i.e. the negative frequency 'image' to the wanted channel. So the wanted channel (at positive frequencies) is now overlapped by this image channel (at negative frequencies). In a similar manner to the zero-IF approach, these overlapping signals can be separated by using a quadrature architecture (I and Q paths), and performing suitable signal processing (complex filtering). An alternative approach would be to instead ensure that the interfering signal at frequency $f_{IM} = f_{LO} - f_{IF}$ is filtered out before reaching the multiplier. However, recall that the wanted channel is f_{IF} above the LO, while the interfering image is f_{IF} below the LO. Since f_{IF} is small, a very sharp filter would be needed in order to pass the wanted channel and reject the image. In practice this is impossible to achieve, and so a low-IF receiver does not reject the image at RF, but instead rejects it at the low IF.

The main disadvantage of the low-IF receiver architecture compared to zero IF receiver architecture is that in zero-IF the interfering signal is the wanted channel itself, while in low-IF the interfering signal is some other channel. The other channel could have a power many times greater than that of the wanted channel, which makes signal recovery much more difficult than in the low-IF case.

It is often very desirable that a particular receiver should be able to receive signals transmitted under a number of different broadcast standards which may have different signal modulation characteristics. As an example, a multi-standard wireless communications receiver may be required to detect and decode new third generation standards such as wideband code division multiple access (WCDMA), while also being capable of receiving signals transmitted under the GSM or DECT standards. It would be highly desirable to have a single receiver integrated circuit capable of handling these different communication standards.

One approach to the design of such a multi-band multi-standard receiver would be to implement a separate receiver structure for each separate broadcast standard, and then integrate each of these parallel receivers into a single integrated circuit. In this way, each separate receiver could be optimised in terms of performance for the particular standard it will receive, for example by selecting the most suitable receiver architecture and circuit implementation. However a significant disadvantage of such an approach is that a large amount of silicon area will be required at high system cost.

The prior art includes attempts to solve this problem. A prior art switchable multi-standard receiver is described in WO02/27953A12. The receiver uses a conventional direct conversion architecture, and comprises three filter stages and three LNA's. The filter stages and the LNA's are selected using switches, depending on the broadcast standard of the incoming signal (e.g. GSM, UMTS or DECT). Common elements of the receiver, a mixer and digital baseband, are connected to each of the outputs of the LNA's. Although the filters and LNA's may be selected for different broadcast standards, the receiver suffers from the disadvantage that the mode of receiver

operation is unchanged, i.e. the mode of operation is always direct conversion, as dictated by the architecture of the receiver.

EP1006669A1 describes a prior art superheterodyne receiver. In this receiver a common LNA and mixer are used for all received broadcast standards. The receiver includes multiple switchable filters, a particular filter being selected to receive a particular broadcast standard and frequency band. Although the filters may be selected for different broadcast standards, the mode of operation of the receiver itself is fixed (i.e. superheterodyne) as dictated by the architecture of the receiver.

The lack of flexibility of receiver mode is a substantial disadvantage. For example in a wireless communications receiver, direct conversion may give a compact and low power solution for the reception of wideband signals such as WCDMA, but direct conversion may be unsuitable for reception of narrowband GSM signals.

A second disadvantage of the prior art is that some redundancy in silicon area remains due to the requirement for multiple versions of a given circuit block, i.e. multiple LNAs and filters are required by the receiver of WO02/27953A12, and multiple filters are required by the receiver of EP1006669A1.

It is an object of the present invention to provide an electric circuit which overcomes at least one of the above disadvantages.

According to the invention there is provided an electric circuit suitable for use as a radio receiver or part of a radio receiver, the electric circuit comprising amplification means, frequency mixer means, and filter means, wherein the filter means is dynamically reconfigurable between a first filter configuration which provides a first operating mode, and a second filter configuration which provides a second operating mode.

The term 'radio receiver' is intended to refer to an electric circuit capable of receiving a radio signal. It is not intended to imply the presence of digital electronics; neither is

it intended to exclude the presence of digital electronics. The filter means may be analogue or digital. The term 'radio receiver' is intended to include an electric circuit which is capable of transmitting signals as well as receiving them, i.e. a transceiver.

The invention is advantageous because it allows the operating mode to be changed, for example in response to a change in a wanted input frequency band or communications standard. This allows the operating mode to be selected for optimal receiving of different broadcast standards.

The invention is very different to the prior art, which provides switching between alternative amplifiers or between alternative filters, but which does not provide switching between operating modes. Since the invention uses reconfigurable filters, rather than switching between alternative filters, the semiconductor area required by a semiconductor implementation of the invention is low.

The filter means may comprise a set of interconnected circuit elements, and the reconfigurability may be provided by switches which modify the interconnections between the circuit elements.

The filter means may comprise a set of interconnected circuit elements, and the reconfigurability may be provided via adjustable bias signals or connections internal to the circuit elements, so as to substantially change their operating point or transfer function.

The first and second operating modes may be variously any of zero-IF, low-IF or heterodyne.

Specific embodiments of the invention will now be described by way of example only, with reference to the accompanying figures in which:
Figure 1 is a schematic illustration of a radio receiver which embodies the invention;
Figure 2 is a schematic illustration of filters of the radio receiver of figure 1;

Figure 3 is a circuit diagram showing a filter which may comprise part of the radio receiver of figure 1;
Figure 4 is a circuit diagram showing an active implementation of the filter of figure 3;
Figure 5 is a circuit diagram showing part of the filter of figure 4;
Figure 6 is a circuit diagram showing an alternative active implementation of the filter of figure 3;
Figure 7 is a circuit diagram showing an alternative filter which may comprise part of the radio receiver of figure 1;
Figure 8 is a circuit diagram showing an active implementation of the filter of figure 7;
Figure 9 is a circuit diagram showing an active implementation of the filters of figures 3 and 7;
Figure 10 is a schematic diagram of an alternative radio receiver which embodies the invention;
Figure 11 is a schematic diagram showing a finite impulse response (FIR) digital filter; and
Figure 12 is a schematic diagram of a further alternative radio receiver which embodies the invention.

A radio receiver which embodies the invention is shown in figure 1. The receiver, which is reconfigurable, comprises an antenna 1, a bandpass filter 2 and a low noise amplifier (LNA) 3. These common elements are connected to two quadrature frequency mixers 4, 5 which are provided with a mixing frequency by a synthesiser 6. Outputs of the quadrature mixers 4, 5 pass to baseband filters 7, 8, and from the baseband filters to amplifiers 9, 10 and analogue to digital converters 12, 13. As is described below, the baseband filters 7, 8 may be interlinked, and for ease of reference may be referred to as a single entity, baseband filters 11, as shown by box 11. The baseband filters 11 can be reconfigured so that the receiver operates in the zero IF mode (i.e. lowpass baseband filters) or in the low IF mode (i.e. complex bandpass filters centred at the low IF).

Figure 2 shows one possible implementation of the reconfigurable baseband filters 11 for zero-IF and low-IF modes. The baseband filters 11 comprise quadrature inputs I_{in}

and Q_{in}, which are connected to lowpass filters 15, 16. Output from a first lowpass filter 15 is passed as feedback via an inverting amplifier 17 and a switch 18 to an input side of the second lowpass filter 16. Similarly, output from the second lowpass filter 16 is passed as feedback via an inverting amplifier 19 and a switch 20 to an input side of the first lowpass filter 15.

When the switches 18, 20 are open, a dual channel lowpass filter is implemented suitable for zero-IF mode operation. When the switches 18, 20 are closed, a complex bandpass filter is implemented suitable for low-IF mode operation. By selecting the switches 18, 20 to be either open or closed, the receiver is may be reconfigured between zero-IF and low-IF modes. In practice a number of the filter arrangements shown in figure 2 could be cascaded to implement a higher-order filter.

The analogue front-end of a typical receiver is usually followed by a digital back-end which provides digital post-processing to perform demodulation and decoding functions.

There are many different ways in which component filters 15, 16, 17, 19 of the baseband filters 11 may be implemented. The type and/or order of the filters themselves may be varied, for example by switching of their constituent components. The reconfiguration of the filters may involve switching of interconnections between the constituent components of the filters, and/or it may involve switching the values of the constituent components (by varying bias values or by switching in additional elements).

An example of a component filter is shown in figure 3. The filter is a doubly-terminated passive ladder filter which implements a fifth-order all-pole lowpass function. Since the ladder filter is passive, its transfer function is fixed. Figure 4 shows an active implementation of a doubly-terminated ladder filter, which has an adjustable transfer function. The implementation of figure 4 is based on active simulation of the filter transfer function, and is suitable for integrated circuit realisation. The filter of figure 4 is constructed from the interconnection of amplifiers

G and integrator sections $1/s\tau$, where various integrator time constants τ determine the pole locations of the filter. By tuning the pole locations (i.e. by varying the integrator time constants), the filter transfer function can be varied, for example from a Chebyshev to a Butterworth response.

Figure 5 shows an integrator configuration which allows easy tuning of the time constant τ. The integrator is a transconductor-capacitor (G_m-C) structure. The value of the transconductance G_m depends on the bias current I_B. By tuning I_B, the integrator time constant changes. Constructing the filter of figure 4 using integrators of the type shown in figure 5 allows convenient variation of the filter transfer function via tuning of the integrators.

An alternative active simulation of the doubly-terminated ladder filter of figure 3 is shown in figure 6. In this circuit the inductors of the passive circuit are simulated using active gyrators formed from transconductors G_m and capacitors C_L. In this instance, the value of a given simulated inductor is determined by the G_m-C elements used to simulate that inductor. To alter the filter response from, for example, a Chebyshev to a Butterworth response, it is not sufficient to simply tune the transconductances of the transconductors, since this will change only the effective inductor values. The values of the capacitors must also be altered. This is achieved by switching in or out additional capacitors C_2, C_4, C_6 using switches S_2,S_4,S_6 as shown in Figure 6.

Figure 7 shows an alternative example of a component filter. The filter is a doubly-terminated passive ladder filter which implements a fourth-order elliptic filter. Figure 8 shows an active implementation of the filter, based upon active simulation of inductor values, which can be implemented on an integrated circuit. The filter of figure 8 is based upon gyrators formed from transconductors G_m and capacitors C_L.

From a comparison of the filters shown in figures 6 and 8 it can be seen that these can be conveniently combined as a single circuit. The combined circuit is shown in figure 9. The configuration of the combined circuit of figure 9 may be varied between

three different settings, (i) lowpass fifth-order Chebyshev, (ii) lowpass fifth-order Butterworth, and (iii) lowpass fourth-order elliptic. This is achieved as follows:

(i) with switches S_{2A}, S_{4A} and S_{6A} shut and all others open, and with transconductors G_{m1}-G_{m4} tuned to appropriate values, the circuit implements a lowpass all-pole filter with particular characteristics, e.g. a Chebyshev response.

(ii) with switches S_{2B}, S_{4B} and S_{6B} shut and all others open, and with transconductors G_{m1}-G_{m4} tuned to appropriate values, the circuit implements a lowpass all-pole filter with a different transfer function to that in (i), e.g. a Butterworth response,

(iii) with switches S_{2C}, S_{3C} and S_{4C} shut and all others open, and with transconductors G_{m1}-G_{m4} tuned to appropriate values, the circuit implements a lowpass elliptic filter.

The filter examples described in relation to figures 3 to 9 are merely illustrative. It will be appreciated that many different filters, different to those in Figures 3 to 9, may be implemented.

Figure 10 shows an alternative implementation of a radio receiver which can be reconfigured between zero-IF mode operation and low-IF mode operation. In this case, the analogue filters are lowpass filters, and the mode reconfiguration is implemented in the digital domain. The receiver comprises an antenna 22, a low noise amplifier (LNA) 23, and two quadrature frequency mixers 24, 25 which are provided with an operating frequency by a synthesiser 26. Outputs of the quadrature mixers 24, 25 pass to analogue bandpass filters 27, 28 and via amplifiers 29, 30 to analogue to digital converters 31, 32. Outputs of the analogue to digital converters 31, 32 pass to reconfigurable digital filters 33.

In operation, when a zero-IF mode of operation is required, the analogue bandpass filters 27, 28 are tuned to the appropriate frequency to allow the wanted channel through, but reject the adjacent channel signal. After the analogue to digital conversion, the digital processing circuitry implements the necessary demodulation

and decoding functions. If the wanted channel is a narrowband signal, the analogue bandpass filters 27, 28 may be configured not to reject all of the adjacent channel signal but merely act as anti-aliasing filters for the subsequent analogue to digital conversion. This will relax the design constraints on the analogue bandpass filters 27, 28 allowing a more compact design. In this case, the digital circuitry after the analogue to digital converter will first perform lowpass channel select filtering prior to demodulation and decoding functions. A suitable lowpass digital filter could be a finite impulse response (FIR) filter with an appropriate number of taps. Figure 11 shows an example FIR filter structure whereby the output signal y(n) is formed from a summation of the weighted outputs of cascaded delay sections (z^{-1}). The transfer function of the filter depends on the number of delay sections (number of taps), and the relative magnitude of the weights h(0), h(1) etc.

If a low-IF mode of operation is required, the analogue bandpass filters 27, 28 are re-tuned (for example by varying the filter bias currents) such that the whole of the baseband bandwidth up to (and including) the wanted channel at the low intermediate frequency (IF) is passed through the analogue bandpass filters 27, 28. The analogue to digital converters 31, 32 will convert the whole of this signal to the digital domain. The digital filters are configured such that they implement complex bandpass filtering, rather than lowpass filtering used in the zero-IF case. For example the FIR structure may be maintained but with modified weights and number of taps. The weight values h(0), h(1) etc. can be changed by updating values stored in digital weight registers, while the number of taps may be increased or decreased by switching in or out additional cascaded delay sections.

An advantage of performing the filter reconfiguration in the digital domain is that digital circuits are easier to reconfigure than analogue circuits, and in addition the complex filters can be implemented with greater matching accuracy (i.e. greater image rejection). However the penalty is a higher ADC conversion bandwidth and thus increased power consumption.

The receiver may be implemented such that both the analogue and digital baseband filters can be reconfigured. In this way, the analogue filters could be fairly narrowband lowpass structures (for a zero-IF receiver), or they may be wideband lowpass filters with complex bandpass filters in the digital domain (for a low-IF digital IR approach); alternatively, the analogue filters may be configured as complex bandpass structures (for a low-IF analogue IR approach). A receiver having reconfigurable analogue and digital baseband filters is shown schematically in Figure 12.

The various circuit blocks such as LNA, mixers, etc may be reconfigured by varying their bias values so as to be optimised for a different frequency band or standard.

The various circuit blocks such as LNA, mixers, etc may also be switchable such that as the baseband is reconfigured, the front-end circuit elements are also switched so as to be optimised for a different frequency band or standard.

Although the described embodiments of the invention are receiver architectures, it will be appreciated that the invention may also be implemented in an architecture in which the integrated circuit front-end is capable of performing a transmitter function, i.e. an RF transceiver architecture.

CLAIMS

1. An electric circuit suitable for use as a radio receiver or part of a radio receiver, the electric circuit comprising amplification means, frequency mixer means, and filter means, wherein the filter means is dynamically reconfigurable between a first filter configuration which provides a first operating mode, and a second filter configuration which provides a second operating mode.

2. An electric circuit according to claim 1, wherein the filter means comprises a set of interconnected circuit elements, and the reconfigurability is provided by switches which modify the interconnections between the circuit elements.

3. An electric circuit according to claim 1 or claim 2, wherein the filter means comprises a set of interconnected circuit elements, and the reconfigurability is provided via adjustable bias signals or connections internal to the circuit elements, so as to substantially change their operating point or transfer function.

4. An electric circuit according to any preceding claim, wherein one of the operating modes is zero-IF.

5. An electric circuit according to any preceding claim, wherein one of the operating modes is low-IF.

6. An electric circuit according to any preceding claim, wherein one of the operating modes is heterodyne.

7. An electric circuit according to claim 2 or any claim dependent thereon, wherein the filter means is provided with quadrature inputs and quadrature outputs, and the switches are arranged to allow feedback to be passed from the quadrature outputs to opposite quadrature inputs.

8. An electric circuit according to any preceding claim, wherein the filter means comprises amplifiers and integrators arranged to simulate a passive filter, the time constants of the integrators being adjustable to adjust the filter means' transfer function.

9. An electric circuit according to claim 8, wherein the integrator is a transconductor capacitor structure having a tuneable bias current

10. An electric circuit according to any preceding claim, wherein the filter means comprises transconductors and capacitors arranged to form active gyrators.

11. An electric circuit according to claim 10, wherein the transconductors are provided with tuneable bias currents, and the capacitors are provided with switches which may be used to switch the capacitors into or out of the filter active gyrators.

12. An electric circuit according to any preceding claim, wherein the filter means implements an all-pole lowpass filter.

13. An electric circuit according to any of claims 1 to 11, wherein the filter means implements an elliptic filter.

14. An electric circuit according to claim 12 and claim 13, wherein the filter means is dynamically reconfigurable between the all-pole lowpass filter implementation and the elliptic filter implementation.

15. An electric circuit according to any preceding claim, wherein the dynamically reconfigurable filter means is implemented in the analogue domain

16. An electric circuit according to any of claims 1 to 6, wherein the dynamically reconfigurable filter means is implemented in the digital domain.

17. An electric circuit according to claim 16, wherein the filter means comprises a finite input response filter with adjustable delay sections and weights.

18. An electric circuit according to claim 15 and claim 16, wherein the analogue dynamically reconfigurable filter means and the digital dynamically reconfigurable filter means are both provided in the electric circuit.

19. An electric circuit substantially as hereinbefore described with reference to figures 1 to 9, figures 10 and 11, or figure 12.

ABSTRACT

An electric circuit suitable for use as a radio receiver or part of a radio receiver, the electric circuit comprising amplification means, frequency mixer means, and filter means, wherein the filter means is dynamically reconfigurable between a first filter configuration which provides a first operating mode, and a second filter configuration which provides a second operating mode.